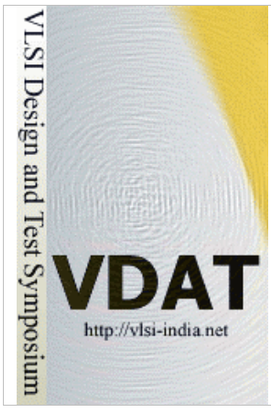

10th IEEE VLSI Design and Test Symposium

VDAT2006

August 9-12, 2006

Venue: International Center, Goa, India

Sponsored by

VLSI Society of India

Industry Sponsors

Texas Instruments India and Controlnet India

In Co-operation with

IEEE EDS/SSCS Bangalore Chapter

IEEE CAS Bangalore Chapter, IEEE –CS-TTTC

IEEE Goa Chapter, Goa University

At a Glance...

Call For Participation

The 10th VLSI Design and Test Symposium (VDAT 2006) will be held at International Centre, Goa; during August 9-12, 2006. You can obtain the information flyer from the Download Section:

- cfp-vdat2006 (PDF)
- Brochure (PDF)
- Travel Details (HTM)
- Hotels at Goa (HTM)
- Venue (HTM)

Important Dates

- Last Date for Paper Submission: March 15, 2006
- Last Date for Tutorial Submission: March 31, 2006
- Notification of Acceptance: May 1, 2006
- Last Date for Sending Final Manuscript: June 1, 2006
- Last Date for Fellowship Application: May 15, 2006
- Full-day Tutorials: August 09, 2006
- VLSI Education Day: August 10, 2006
- Symposium Dates: August 09-12, 2006

Technical Tracks

VDAT symposium runs in three concurrent technical tracks:

1. **Track on High-level Design** will discuss issues related to system-level synthesis, microarchitecture, embedded systems, codesign, core-based design of SoC, timing convergence, high-level synthesis, logic synthesis, memory synthesis, and FPGA synthesis.
2. **Track on Physical Design and VLSI Technology** will discuss all issues related to physical design and process related aspects of integrated circuits, such as layout, fabrication, packaging, opto-electronic circuits, MEMS, deep submicron and nanometer devices.
3. **Track on Testing and Verification** will discuss issues related to testing, testability, and verification of digital designs, memories, analog designs, and mixed-signal designs, and circuits containing deep-submicron and nanometer devices.

Technical Paper Presentations

The last date for Paper Submission has now passed. If you have submitted a paper, you will shortly hear about our decision about the paper-review and selection!

Information for authors of VDAT 2006

Tutorials & Panel Discussions

Details of tutorials will become available by June 2006. Three parallel tutorials T1, T2, and T3 will be run.
If you have submitted proposals for embedded tutorials (1 hour or 2 hour duration), full-day and half-day tutorials, you will shortly hear from us about our decision.

We invite proposals for panel discussions.
The proposal must include an extended abstract, the agenda and profiles of the speakers.

Get Involved!

We invite your ideas and suggestions for making VDAT 2006 symposium a memorable experience to all. It could be setting up of University Booths or putting up of Industrial Exhibits. There could be proposals for best paper awards, proposals for panel discussions, proposals for design contests, or even proposals for sponsorships! Participants can contribute their ideas, for making the Symposium an enriching experience for all. Please express your ideas to us!

Ideas, Suggestions and Proposals

Corporate sponsors and exhibitors must contact the *General Chairs* for details of sponsorship.

Symposium Committee

General Co-Chairs

C.P. Ravikumar, Texas Instruments India
P. Sridhar, Controlnet India

Technical Program Committee

Vishwani Agrawal, Auburn University, USA
Bharadwaj Amruthur, Indian Institute of Science
P.V. Anandmohan, ECIL, Bangalore
Shabbir Batterywala, Synopsys, India
Navakanta Bhat, IISc, Bangalore, India
Bhargab Bhattacharya, ISI Calcutta, India
Srimat Chakradhar, NEC, USA
N. Chandrachoodan, IIT Madras
V. Kamakoti, IIT Chennai, India
R. Koodli, Infineon Technologies, India
Preeti Ranjan Panda, IIT Delhi, India
S. Mahant-Shetti, KARMIC, India
Nilanjan Mukherjee, Mentor Graphics, USA
D. Nagchoudhuri, DAIICT, Gujrat, India
S. Natarajan, Emerging Memory Tech., Canada
R. Parekhji, Texas Instruments, India
C.P. Ravikumar, Texas Instruments, India
Partha Ray, National Semiconductor, India
J.N. Roy, Punjab University, India
Vineet Sahula, MREC Jaipur
Dinesh Sharma, IIT Bombay, India
S. Srinivasan, IIT Madras, India
Susmita Sur-Kolay, ISI Calcutta
Laxman Vemury, Silicon Image, USA
V. Visvanathan, Texas Instruments, India

Local Organization Chairs

Satish Kenkre, Controlnet India

Organizing Committee

P. Sridhar ControlNet
Rashid Kukkady, Controlnet
Satish Kenkre, Controlnet
Praveen K Saxena ControlNet
V.V. Kamat, Goa University
Shailendra Aswale RIT, Shiroda
Olavo D'Seuza PCCE, Goa
Nilesh F Dessai GEC, Farmagudi
Komala Soares PCCE, Goa
MK Deshmukh, BITS, Goa

Website

Yashdeep Mahajani, Wipro, India

Fellowships Chair

Narasimha Kaulgud, Wipro
vdat06fellow@hotmail.com

Finance Chair

Gopal Naidu, Texas Instruments India
vdat06-regn@hotmail.com

Registration Information:

- Registration permits you to participate in all the Technical sessions and Tutorials organized as part of the Symposium, and includes refreshments and lunch on all days.
- Please send your registration fee through a draft made out to "*VLSI Design and Test Symposium, 2006",* payable at Bangalore*.*
- The draft must be sent to *Mr.Gopal Naidu, Finance Chair (VDAT 2006), Texas Instruments India, Bagmane Tech Park, C.V. Raman Nagar, Bangalore 560093.*
- If you wish to register *on the spot*, drafts and cash payment in Indian rupees are acceptable. We will not be able to accept Foreign Currency or Credit Card payments.
- The current exchange rate is approximately 1 US dollar = 45 Indian rupees.
- Even those of you who plat to register on the spot are requested to communicate your desire to attend VDAT 2006 to vdat06@hotmail.com with details of vehicle registration number (if any) and laptop number (if any). Without this, you may face difficulties during registration. Please mark the subject line of the mail as "Vehicle No." or "Laptop No."
- If you are registering for a tutorial, indicate the first and second preference of the tutorial. There are limited seats in each tutorial. If we cannot register you in the tutorial of your choice, we will refund the amount.
- A processing fee of Rs.500/- will be applied against all cancellations.

Symposium Registration Amount

	Fellow	Indian Faculty/ Student	Indian Industry VSI/ IEEE Member	All Foreign Participants	Others
Before June 30, 2006	Rs.1500/=	Rs.2500/=	Rs.6000/=	US$ 150.00	Rs.7000/=
After June 30, 2006	N/A	Rs.3000/=	Rs.7000/=	US$ 200.00	Rs.8000/=

Tutorial Registration Amount

Before June 30, 2006	Rs.1000/=	Rs.1500/=	Rs.2000/=	US$ 100.00	Rs.2500/=
After June 30, 2006	Rs.1500/=	Rs.2000/=	Rs.2500/=	US$ 125.00	Rs.3000/=

Correspondence address for Registration:
Mr. Gopal Naidu
Finance Chair, VDAT2006
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park, Opp. LRDE
C.V.Raman Nagar, Bangalore – 560 093
FAX: 91-80-25048213
vdat06-regn@hotmail.com

Information

*Please watch updates on VDAT at http://vlsi-india.net The idea behind the VLSI Design And Test (VDAT) Symposium is to promote Research and Development on all aspects of VLSI in India. This symposium is a forum for free discussion of hot and emerging topics in VLSI. It provides a meeting place for VLSI professionals working in India and abroad. We have been holding this event since 1998, and the participation in the event has steadily gone up every year. Until 2004, the event was called "**VLSI Design and Test Workshops**." The VLSI Industry in India and academic community working in the area of VLSI has provided immense support to the symposium.*

*VDAT is sponsored by the **VLSI Society of India**. Please consult http://vlsi-india.net/vsi for more information on VSI''s mission and goals. If you are unable to download the page, please send mail to vsisecy@vlsi-india.net for a softcopy of the application form.*
Consult http://www.vlsi-india.net/vsi/activities/ for updates on the activities of the VLSI Society of India. If you wish to become a member of the VLSI Society of India, you can download the form from http://vlsi-india.net/vsi/membership/.

Paper Submission

ADDRESS FOR CORRESPONDENCE

Proposals for one-day tutorials are invited. Each proposal must include an extended abstract, the agenda, and profiles of the speakers. Tutorials targeting Post Graduate students, faculty, and professionals with up to 2 years experience will be given higher priority.

Authors should submit full papers of **at most 10 A4-size pages, including figures and references**.
Submissions will undergo blind review – the authors must not include their names or affiliations in the submissions.
Your submission should represent original contribution and should not have been submitted to other forums.
It is important that abstracts bring out the contribution and novelty of the paper.
Survey papers are not acceptable as submissions. However, proposals for embedded tutorials (1 hour or 2 hour duration), full-day and half-day tutorials, and proposals for panel discussions are invited.
Please indicate clearly in the submission that your submission is a proposal for an embedded tutorial.
Send your submissions through the Docman system accessible from www.vlsi-india.net as well as http://vlsi.nj.nec.com/

For questions relating to technical program, submissions, and sponsorships, write to:

Dr C. P. Ravikumar

Texas Instruments, India

Bagmane Tech Park, CV Raman Nagar,

Bangalore 560093

Email: cpravikumar@hotmail.com

FAX: 91-80-25048213

Submitting authors must become members of the vdat@yahoogroups.com mailing list, where updates on the symposium will be sent. Registration form and information about the local arrangements will be available from www.vlsi-india.net after March 1. Send any queries only to vdat06@hotmail.com

Paper Reviews

Conference Management Toolkit

On-line paper submission/review for VDAT Symposium is managed by CMT (Conference Management Toolkit). Please use the following link for making paper submissions to VDAT 2006:

https://msrcmt.research.microsoft.com/VDAT2006/
Click on "User Login." You may need to create your login ID and profile by clicking "New User Registration". The instructions are self-explanatory.

If you are a reviewer, you can log-into the system by clicking on the link here:
https://msrcmt.research.microsoft.com/VDAT2006/reviewer

For general questions or concerns about CMT usage, please refer the FAQs, available here:

FAQs for Authors:

FAQ for authors at CMT	https://msrcmt.research.microsoft.com/cmt/faq/faq_author.asp
CMT issues and solutions	https://msrcmt.research.microsoft.com/cmt/faq/faq_author_error.asp
General information about phases in CMT usage	https://msrcmt.research.microsoft.com/cmt/faq/faq_author_phase.asp

FAQs for Reviewers:

FAQ for reviewers at CMT	https://msrcmt.research.microsoft.com/cmt/faq/faq_reviewer.asp
CMT issues and solutions	https://msrcmt.research.microsoft.com/cmt/faq/faq_reviewer_error.asp
General information about phases in CMT usage	https://msrcmt.research.microsoft.com/cmt/faq/faq_reviewer_phase.asp

If you have difficulties in submission please let us know

TITLE: HOW TO TYPE-SET YOUR PAPER FOR VDAT 2006 PROCEEDINGS

Author: Elite Publishers[1]

Abstract

This document provides instructions to authors of papers accepted for presentation in the seventh VLSI Design and Test Symposium to be held in Goa during August 09-12, 2006. This is a hard deadline. Manuscripts arriving later will not be published in the hardcopy proceedings. Please follow the following format guidelines carefully. Author(s) are required to compose the text, drawings, photographs, tables and slides within the range of print area (4.5" X 8"). This document has been typeset using the directions that you will find below.

1. Page Formatting and Page Limit

Regular papers and embedded tutorials will have a limit of 10 pages, short papers will have a limit of 8 pages. Authors have the option of buying at most two extra pages by paying Rs. 1000/- per page. Send the cheque to Mr Gopal Naidu, Finance Chair, VDAT 2006, Texas Instruments (India) Pvt Ltd, Bagmane Tech Park, Opposite LRDE, C. V. Raman Nagar Post, Bangalore - 560093; and make the draft payable to "VLSI Design and Test Symposium 2006." At the back of the DD, please write "*For extra pages in VDAT 2006 proceedings.*"

2. Paper (Text matter)

Final manuscript must be submitted by e-mail to vdat06@hotmail.com no later than June 20, 2006. Papers must be formatted using MS Word format. We are sorry, we cannot accept PDF, PS, or other formats. The manuscript should be typewritten in single line spacing and standard font spacing, with 10 points font size in Times New Roman script. The VDAT proceedings is published in the form of a book and he page size is smaller. You must use MS/Word and go to the File-> Page Setup menu and adjust the margins such that the print area is 4.5" wide and 8" in height. Please use a single column.

3. Presentation

Abstract, introduction, sub-headings, paragraphs and conclusions of the manuscript should begin at the left margin and should be consistent throughout the paper.

4. Arrangement of the Manuscript

The manuscript should contain following points arranged in the order specified below:

4.1 Title

The Title of the paper shall be typewritten in **BOLD CAPITAL LETTERS** with center justification at the third line of the first page in 16-points size.

4.2 Name(s) of the Author(s), Title(s) and Affiliation

Typewrite the name of the author(s) in bold 12-points font size followed by their title(s). Leave one line space in between the title of the paper and the name of the author(s). Print affiliation of the Author(s) in 9 points front size in footnotes.

4.3 Abstract

Synopsis of not more than 200 words should be written on a new paragraph leaving one line space after the name(s) of the author(s). Use 10-points font size. The abstract should clearly focus on the scope of the paper and the main conclusions reached.

4.4 Keywords (Index)

List out key words in Italics and 10 points size.

4.5 Tables and Figures

All graphic items must fit within the print area. Lettering within the tables and figures should be 10 points. Please do not use color in your figures or any part of the manuscript. If you plan to include an image, ensure that it is of high quality so that when printed it will reproduce clearly. All figures and tables must have captions and must be numbered.

4.6 Sections

Number your sections 1, 2, 3, etc. and subsections 2.1, 3.2.1, etc.

4.7 References

Within the text references should be indicated by citing the surname of the author(s) followed by the year of publication. The abbreviated author and date references should be placed in parentheses when citing a reference, e.g Abdulla, Ravikumar and Ashul Kumar (1998), or Cheng and Agrawal (1993). Here is a sample reference:

[1] Contact Information: Elite Publishers, New Delhi. Rg_elite@yahoo.com

[1] M.F. Abdulla, C.P. Ravikumar and Anshul Kumar (1999). *Built-in Self Test based on Multiple On-chip Signature Checking*. Journal of Electronic Testing: Theory and Applications, Kluwer Publishers, 1999, 227-244.

5 Slides

Authors must submit the presentation foils in Power Point format (PPT) no later than July 20, 2006. We will get the foils reviewed by the session chairs and as a result, the foils are needed earlier. Please use at least 36 points for titles of the slides and at least 18 point font size for the text in your slides.

6 Copyrights

Any necessary rights or permission to reproduce quoted material or illustrations published elsewhere remain the responsibility of the author(s). To Safeguard authors' right, the copyright of all material published in the proceeding is vested in the publisher.

7 Submission

Submit the final camera-ready version at CMT and if unsuccessful in log-in, electronically to vdat06@hotmail.com

References

[1] M.F. Abdulla, C.P. Ravikumar and Anshul Kumar (1999). *Built-in Self Test based on Multiple On-chip Signature Checking*. Journal of Electronic Testing: Theory and Applications, Kluwer Publishers, 1999, 227-244.

Appendix A: MS Word Setting

We recommend the following procedure when you use MS/Word to typeset your document. Go to File-Page Setup menu and select paper size to be Letter (8.5” x 11”). Then set margins as follows – top and bottom margins of 1.5”, and left and right margins of 2” each. Set gutter to 0” and header and footer margins to 0.5”.

Registration

Registration of Participants

Symposium registration permits you to participate in all the technical sessions and tutorials organized as part of the symposium. Refreshments and lunch will be provided to all registrants at no extra charge. Transport and stay arrangements are the responsibility of the participants.

Advance Registration

If you wish to register in advance, please send the duly filled registration form along with the registration fee through a draft made out to "*VLSI Design & Test Symposium 2006*". Make the draft payable at Bangalore. The draft must be sent to the Finance and Registration Chair

Click here to download the registration form:

Registration Form

On The Spot Registration

Even those of you who are thinking of registering on the spot are requested to communicate your desire to attend VDAT 2006 symposium to the Finance and Registration Chair in the following proforma.
Registration Form

Without this, you may face difficulties during registration. If you wish to register on the spot, drafts and cash payment in Indian rupees will be acceptable. We will not be able to accept foreign currency or credit card payments.

Registration Charges

The registration fees for symposium will be charged as given below:

Symposium Registration Amount		
	Before June 30, 2006	**After June 30, 2006**
Fellow	Rs 1500	N/A
Faculty/ Student	Rs 2500	Rs 3000
Indian Industry VSI/ IEEE Member	Rs 6000	Rs 7000
Foreign Participant	USD 150	USD 200
Others	Rs 7000	Rs 8000

Full-day tutorials will be held on August 09, 2006. There are limited seats in each tutorial. The registration fees for the tutorials will be charged as given below:

Tutorial Registration Amount		
	Before June 30, 2006	**After June 30, 2006**
Fellow	Rs 1000	Rs 1500
Faculty/ Student	Rs 1500	Rs 2000
Indian Industry VSI/ IEEE Member	Rs 2000	Rs 2500
Foreign Participant	USD 100	USD 125
Others	Rs 2500	Rs 3000

If you are interested in a day trip to Doodh Sagar Falls trip (on August 13, 2006), please add the following charges to your registration amount. The details of the trip are available here.

Trip to Doodh Sagar Falls	
Per participant	Rs 500

For any queries regarding registration, feel free to write to: *mailto:vdat06-regn@hotmail.com*

Venue

About the venue

Goa is known for its beaches with plenty of silicon and pleasant, relaxing atmosphere. The symposium venue is the International Centre located at the tranquil Dona Paula, near Goa University. The location details are as follows:

The International Centre,
Goa University Road,
Dona Paula,
Goa - 403 004,
INDIA

website: *www.internationalcentregoa.com*

International Centre, Goa (ICG) is a non-profit Institutional Society, which provides a stimulating environment for generation of ideas, a fertile ground for appreciating beauty in all cultures and an ambience for relaxation.

Travel and Accommodation

Useful information about traveling to the Symposium venue is available here:

Travellers Guide

Panjim is about 5 km from the venue and has several hotels at costs varying from Rs 500/- per day and upward. Off-season discounts will be available at most hotels. Upscale hotels include Marriot in Panjim and Cidade De Goa in Dona Paula. Details about some selected hotels are available here:

List of Selected Hotels

Please note that the VDAT 2006 organizing committee will not make arrangements for residential accommodation of the participants.

Trip to Doodh Sagar Falls

A day trip to *Doodh Sagar Falls* will be arranged by the organizers on August 13, 2006 (Sunday), if there is sufficient interest. The cost of the trip will be Rs 500/- inclusive of lunch and ticket. The picnic party starts at 6.00 AM and will return at 7.00 PM.

Please indicate your interest about this trip in your registration form.

The Weatherman Says...

During August, Goa witnesses the monsoon season.

The main feature of the Goan climate is the monsoon, which occurs between June and the end of September. This period is considered to be out of season as the South West Monsoon starts in June and brings heavy rainfall of up to 3 ½ metres over the next 3 months.

This time of the year finds Goa at its most colorful with emerald green paddy fields and plants growing before your eyes.

Glimpses of Goa

Courtesy: Amey Hegde, Wipro Technologies, Bangalore

Travel Information

Travel from Dabolim Airport to Goa University

Kms: **29 kms**
Mode of Transport: Airways
Source: Mumbai / Bangalore
Dest: Goa (Dabolim Airport)

Type of Vehicle	Price (Rs.)
Ordinary Taxi (Maruti Van,Ambassador)	Rs.480
Luxury Taxi	Rs.800(OneWay trip)*
(Accent,Bolero)	Rs1000(Half-Day Hire)* Rs.1400 (Full-Day Hire)*

Public Transport	Price (Rs.)
Route I	Dabolim Airport-Chicalim Junction -Panaji-GU Rs.4(Private Bus) from Airport to Chicalim Junction Rs.12(KadambaBus) from Chicalim Junction-Panaji
Route II	Dabolim Airport -Verna Circle -Panaji Rs.6 (Private Bus) from Airport-Verna Circle Rs.10 (KadambaTransport) from Verna Circle - Panaji
Route III	Dabolim Airport-Vascodagama(KTC Bus Stand)-Panaji Rs.4(Private Bus)Dabolim Airport-Vascodagama(KTC Bus Stand) Rs.12(Kadamba Transport)Vascodagama(KTC Bus Stand)-Panaji
Route IV	Dabolim Airport-Vascodagama(Old Bus Stand)-Panaji Rs.4(Private Bus)Dabolim Airport-Vascodagama(Old Bus Stand) Rs.15(Kadamba Non-Stop Bus)Vascodagama(Old Bus Stand)-Panaji

Source	Destination	Distances in Kms
Airport	Vascodagama	3
Airport	Panaji	29
Airport	Verna Circle	7
Vascodagama	Verna Circle	10
Vascodagama	Panaji	30

Flight Arrivals(Airport)	FROM	Time
IC-663	Mumbai	620
DN-317	Mumbai	650
9W-479	Mumbai	730
9W-475	Mumbai	1300
IT-306	Mumbai	1300
S2-219	Mumbai	1305
IC-865	Mumbai	1355
G8-105	Mumbai	1440
DN307	Mumbai	1515
9W-473	Mumbai	1535
IC-163	Mumbai	1530
OS259	Mumbai	1715
G8-101	Mumbai	1750
IC-919	Bangalore	1405
9W-3525	Bangalore	1430
IT424	Bangalore	1500
DN305	Bangalore	1540

* SUBJECT TO CHANGE (Depending upon Fuel Hike,Tourist Season)

Travel from Karmali Railway Station To Goa University

Kms: **19**
Mode of Transport: Railways
Source: Mumbai
Dest: Goa (Karmali Railway Station)

Vehicle Type	Cost (Rs.)
Taxi (Maruti Van,Ambassador)	265

Trains Arrival To Goa (Karmali Railway Stn)	Source	Arrival Time
Konkan Kanya Express (Leaves MUMBAI: 23:00)	MUMBAI	9:45
Netravati Express(Leaves MUMBAI: 11:40)	MUMBAI	21:45
Mandovi Express(Leaves MUMBAI: 06:55)	MUMBAI	17:35

Travel from Panjim Bus Station To Goa University

Kms: **8**
Mode of Transport: Roadways
Source: Mumbai / Bangalore
Dest: Goa (Panjim Bus Station)

Vehicle Type	Cost (Rs.)
Taxi (Maruti Van, Ambassador)	150
Public Transport	6

Bus Arrival To Goa (Panjim Bus Stn)	Source	Arrival Time	Cost(Rs.)
Volvo Sleeper	MUMBAI	8:30	700
Volvo Seater	MUMBAI	6:30	600
Volvo	MUMBAI	7:00	500

Bus Arrival To Goa (Panjim Bus Stn)	Source	Arrival Time	Cost(Rs.)
Volvo Sleeper	BANGALORE	10:30	750
Volvo Seater	BANGALORE	10:30	650

Travel from Margao Railway Station To Goa University

Kms **37**
Mode of Transport: Railways
Source: Mumbai / Bangalore
Dest: Goa (Margao Railway Station)

Vehicle Type	Cost (Rs.)
Taxi (Maruti Van,Ambassador)	480

Trains Arrival To Goa (Margao Railway Stn)	Source	Arrival Time
Konkan Kanya	MUMBAI	10:30
Netravati Express	MUMBAI	22:30
Mandovi Express(Leaves MUMBAI: 06:55)	MUMBAI	18:00

Trains Arrival To Goa (Margao Railway Stn)	Source	Arrival Time
Yashwantpur (MON, SAT)	BANGALORE	8:30

Travel from Margao Bus Station To Goa University

Kms **34**

Mode of Transport: Roadways

Source: Mumbai / Bangalore

Dest: Goa (Margao Bus Station)

Vehicle Type	Cost (Rs.)
Taxi	450
(Maruti Van,Ambassador)	
Public Transport	12
Public Transport (Shuttle Serv)	17

Bus Arrival To Goa (Panjim Bus Stn)	Source	Arrival Time	Cost (Rs.)
Volvo Sleeper	MUMBAI	8:30	700
Volvo Seater	MUMBAI	6:30	600
Volvo	MUMBAI	7:00	500

Bus Arrival To Goa (Panjim Bus Stn)	Source	Arrival Time	Cost (Rs.)
Volvo Sleeper	BANGALORE	10:30	750
Volvo Seater	BANGALORE	10:30	650

Hotels at Goa

List of selected hotels at Panaji, Goa:

Name of the Hotel	Address	Std. Non A.C.	Std. A.C.	Dbl. Non A.C.	Dbl. A.C.	Single Dlx. Exe.	Dbl. Dlx. Exe.	Single A.C. Suite	Double A.C. Suite
Hotel Nova Goa	Dr.Atmaram Borkar Rd.,Panjim Email: novagoa@sancharnet.in Ph: (0832) 2226231-2 Fax: (0832) 2224958		1700/-		2300/-	2000/-	2700/-	2800/-	3300/-
Hotel Mandovi	D.B.Bandodkar Rd.,Panjim Email:mandovi_goa@sancharnet.in Ph: (0832) 2224405-09 / 2436979 Fax: (0832) 2225451		1800/-		2200/-	3250/-	3650/-	4500/-	5500/-
Hotel Delmon	Caetano Alobuquerque Rd, Panjim Email: delmon@sancharnet.in Ph: (0832) 2226846/7, 2420075 Fax: (0832) 2223527	1000/-		1800/-		1500/-	2000/-		
Hotel Manoshanti	Dr. Dada Vaidya Rd., Behind EDC, Panjim Email: dhond@sancharnet.in Ph: (0832) 2224824 / 2421786 Fax: (0832) 2220654				1050/-			1200/-	
Hotel Park Plaza	Opp. Azad Maidan , Panjim parkplaza@sancharnet.in Ph: (0832) 2422601-3 / 2463796 Fax: (0832) 2225635	1200/-	1500/-	1500/-	2000/-			2000/-	2500/-
Hotel Fidalgo	18th June Rd.,Panjim Email: jukfidalgo@yahoo.com info@hotelfidalgo-goa.com Ph: (0832) 2226291-99 / 248101-10 Fax: (0832) 2225061		2300/-		2800/-	2100-2800/-	2600-3300/-		5000-8000/-

Please note that the VDAT 2006 organizing committee will not make arrangements for residential accommodation of the participants.

Fellowships

Every year, VDAT offers fellowships to teachers and research scholars from educational institutions from India to attend the VLSI Education Day and VLSI Design and Test Symposium.

A fellowship should not be viewed as an honor or recognition. It should be viewed as an encouragement to attend VDAT when the participant lacks financial support from the academic institution he/she belongs to. Please do not apply for fellowship if your organization can support you or if you can support yourself.

Fellowships only involve a subsidized registration fee. No other support will be available. Travel and stay arrangements must be made by the participants.

If you are granted fellowship, you are expected to attend the event on all days. There will be no exception to these rules.

Eligibility

If you are a postgraduate student from India specializing in VLSI or a faculty member from India, working in the areas related to VLSI, you can apply for a full or partial fellowship. If you are an undergraduate student who has submitted a paper to VDAT, you are also eligible for a fellowship.

The applicant must be a student or a faculty at the time of the symposium. If you are a graduating student who will not have student status during August 2006, you are not eligible for fellowship.

Selection Criteria

We consider several criteria to shortlist the fellows. Our criteria includes:

- Maximum limit on fellowships and trying to ensure all geographic areas of India are represented in a fair manner
- Completely filled application with letter from Head of the Department sent in hardcopy before the deadline
- Priority for faculty working in VLSI area
- Priority to authors of submitting papers - we have limited to one per paper when multiple authors have applied for fellowship
- Priority to PG students pursuing M.Tech in VLSI
- Priority to faculty who have not received fellowships before to attend VDAT

Application Procedure

Applications must be forwarded in the proforma given below, by email to the Fellowships Chair, no later than May 15, 2006.
Fellowship Application Form (PDF Format)

Attach your bio-data with the application form. Please have your application forwarded by your HOD or Principal of your Institute.

Decisions about grant of fellowship will be made available on this web site. If you are granted fellowship, you are expected to register with full amount before June 30, 2006 and attend the event on all days.

Contact Us

Publications and General Co-Chair

Dr C. P. Ravikumar
APDC, Texas Instruments (India) Pvt Ltd,
Bagmane Tech Park, Opposite LRDE,
C.V. Raman Nagar Post,
Bangalore - 560 093
Email: *cpravikumar@hotmail.com*

Local Organization Chair

Satish Kenkre
ControlNet (I) Pvt. Ltd.
U-1, L-44, STPI,
Verna, Goa 403722, India.
Phone: +91-832-2883601
Fax: +91-832-2783614

Fellowships Chair

Dr Narasimha kaulgud
WIPRO Technologies,
No 72., Keonics Electronics City,
Hosur Main Road,
Bangalore - 561 229
Email: *vdat06fellow@hotmail.com*

Finance and Registration Chair

Mr Gopal Naidu
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park, Opposite LRDE,
C.V. Raman Nagar Post
Bangalore - 560 093
Email: *vdat06-regn@hotmail.com*

Website

Suggestions regarding the website may be sent to: webmaster@vlsi-india.net

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VDAT Symposium is supported each year by several leading companies from the VLSI, Embedded, Silicon and EDA industries. If you would like to become a corporate supporter of VDAT 2006 symposium or if you would like to put up an Industry Exhibit at the Symposium Site, please contact the General Chair (*Dr C. P. Ravikumar*) for details of sponsorship.

VDAT Mailing Group

A mailing group is setup at http://groups.yahoo.com/group/vdat to provide information about the VLSI Design and Test symposium that is held in India every August. In addition, information about other similar events taking place in India or abroad is also disseminated through this mailing list.

You may use vdat@yahoogroups.com to publicize events related to VLSI Design/EDA/Test that take place in and around India. You can also use this address to discuss/debate issues related to VLSI in India.

The list owner of the VDAT mailing group may be contacted at: vdat-owner@yahoogroups.com.

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VLSI Design and Test Symposium

VDAT

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10th IEEE VLSI Design and Test Symposium

August 09 - 12, 2006, Goa, India

Website: www.vlsi-india.net

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FELLOWSHIP APPLICATION FORM

Name of the Fellowship Applicant: (Please use block letters.)

Address for Correspondence:

Designation: Student ☐ **/** Faculty ☐

(You should be a student or a faclty member at the time of Symposium to avail fellowship – Otherwise, the fellowship stands cancelled.)

College/ Institute Name:

Institution and Departmental Address:

E-mail: (Compulsory):

Telephone:

Experience in VLSI Field: (Teaching/Projects)

Is your parent institution ready to partially support you?	Yes ☐ / No ☐
Have you submitted a paper to VDAT 2006?	Yes ☐ / No ☐
Have you received a Fellowship to attend VDAT before?	Yes ☐ / No ☐

Signature

- Email the completed application form to the following address:
  Dr Narasimha Kaulgud,
  Fellowship Chair, VDAT 2006
  Email: vdat06fellow@yahoo.co.in
- Attach your Bio-data with this form. Please have your application forwarded by your HOD or Principal of your Institute. Send the form to reach the Fellowships Chair through e-mail by **May 15, 2006**.
- Queries regarding fellowships must be sent only to: vdat06fellow@yahoo.co.in

- If you are granted fellowship, you are expected to register with full amount before **June 30, 2006** and attend the event on all days.
- Queries regarding registration must be sent only to: vdat06-regn@hotmail.com

Note: A fellowship should not be viewed as an honor or recognition, but as an enabler to attend VDAT for students/faculty who do not get adequate support. Please do not apply if your organization can support you or you can support yourself. Fellowship entitles you to a lower registration fee. No other support will be available.

10th IEEE VLSI Design and Test Symposium

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REGISTRATION FORM

Name of the participant: (Please use block letters.)

Category: (Tick appropriate)	Fellow	☐	VDAT 2006 Fellowship No:
	Faculty / Student	☐	
	Indian Industry VSI/ IEEE member	☐	VSI/ IEEE Membership No:
	Foreign Participant	☐	
	Others	☐	
Address for Correspondence:	**Designation:** Student ☐ Faculty ☐ Industry ☐ Other ☐ **College/ Company Name:** **Permanent address:**		
E-mail: (Compulsory):			**Telephone:**
Choice of tutorial:	**T1** ☐ **/ T2** ☐ **/ T3** ☐		
Details of DD enclosed	Total Amount:		DD Number:
	Drawn on Bank:		Dated:
Are you interested in Doodh Sagar Falls Trip on August 13, 2006? If yes, please include Rs 500/- for trip.	**Yes** ☐ **/ No** ☐		Signature

Tutorial Registration Amount

	Before June 30, 2006	*After June 30, 2006*
Fellow	Rs 1000	Rs 1500
Faculty/ Student	Rs 1500	Rs 2000
Indian Industry VSI/ IEEE Member	Rs 2000	Rs 2500
Foreign Participant	USD 100	USD 125
Others	Rs 2500	Rs 3000

Symposium Registration Amount

	Before June 30, 2006	*After June 30, 2006*
Fellow	Rs. 1500	N/A
Faculty/ Student	Rs.2500	Rs 3000
Indian Industry VSI/ IEEE Member	Rs. 6000	Rs. 7000
Foreign Participant	USD. 150	USD 200
Others	Rs, 7000	Rs.8000

Mail the completed registration form and DD to the following address:

Mr. Gopal Naidu
Finance Chair, VDAT 2006
Finance Department
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park
C.V. Raman Nagar, Bangalore 560093
Email: *vdat06-regn@hotmail.com*

- *The DD to be made out to "**VLSI Design and Test Symposium 2006**" payable at **Bangalore**.*
- *Queries regarding registration must be sent only to:* *vdat06-regn@hotmail.com*
- ***Venue:*** The International Centre, *Goa University Road, Dona Paula, Goa - 403 004, INDIA*

Note: Symposium registration fee includes registration material, lunch and refreshments on all the days. Transport and stay arrangements are the responsibility of the participants.

VLSI Society of India

Registered Society under KSR Act 1960, Rule 1961

Website: http://vlsi-india.net/vsi E-mail: **vsi_india@rediffmail.com**

Membership Form

For new membership and renewals.

New Members to affix photograph.

1. Existing Membership No: ☐☐☐☐ (Quote additional Old No. If any): ☐☐☐☐

   Member (tick as applicable): ☐ **Student** / ☐ **Non-student** / ☐ **Corporate**

2. Your Name:

3. Your Profession/ Designation:

4. Your e-mail address:

5. Your Contact address:

6. Your Professional address (if different from above):

7. Your Area of specialization:

8. Would you like to review papers in events organized by VSI? :

9. How many papers are you willing to review? :

10. Your Brief bio-data: Attach separately

11. How can you contribute to the activities of VSI? :

12. What Activities would you like VSI to organize? :

13. Details of Payment:

Cash/ Credit Card	
DD no:	
Dated:	
Drawn on Bank:	
Amount:	

I agree to be a member of the VLSI Society of India and have read and understood the charter of the society. I will actively contribute towards the objectives of the society.

Place and Date: **Member Signature**

Category	**Membership Rates:**	
	Yearly	**5-yearly**
Student Member:	Rs. 500/=	N/A
Non-student member:	Rs. 1,000/=	Rs 4,500/-
Corporate member:	Rs. 10,000/=	Rs 45,000/-

The DD to be made out to: "VLSI Society of India" and payable at Bangalore.
Mail the form along with the DD to:

Mr. Gopal Naidu
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park, Adjacent to LRDE, C.V.Raman Nagar Post, Bangalore: 560 093
(FAX: 91-80-25048213)

General Note:	Please allow two weeks to process. Students to attach College credentials signed by the authorities. Non-student members to indicate company/ institution name. For renewals, remember to quote your existing membership number. You can mail payment details to vsi_india@rediffmail.com when you send DD by post/ courier. Visit our Download section http://203.200.181.210/index.php?dir= for details on VSI activities. Please notify change of address. You can become a member of VDAT Mailing group for information on VSI and other VLSI related activities in India and abroad. For subscribing: vdat-subscribe@yahoogroups.com To unsubscribe: vdat-unsubscribe@yahoogroups.com

We would like to hear from you!

Tell us what you think about the VDAT symposium, VLSI Education Day, our web site, or anything else that comes to mind. If you have any queries about fellowships, university booths, paper presentations, technical programme details, awards, sponsorships, etc, please use this form to channel them to the right people. Go ahead! Send your questions, comments and feedback. We welcome all of them.

Comments on VDAT 2006

Tick appropriate

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If other, please specify:

Enter your comments in the space provided below:

Tell us how to get in touch with you:

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You can print this page, fill-up and Fax (91-80-25048213) or copy and e-mail the filled up form to cpravikumar@hotmail.com